REMARKS

Reconsideration of the application is requested.

Applicants acknowledge the Examiner's confirmation of receipt of applicants' certified copy of the priority document for the German Patent Application 100 63 627.6, filed December 20, 2000 supporting the claim for priority under 35 U.S.C. § 119.

Claims 1-10 and 12-21 remain in the application. Claims 1, 4, 9, 10, 12, and 15 have been amended. *Claims 11 and 22 have been canceled to facilitate prosecution of the instant application.*

In "Claim Rejections - 35 USC § 112" items 1-3 on page 2 of the above-identified Office Action, claim 4, 9, and 10 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that there is insufficient antecedent basis for the limitation "said processing unit" in the claims.

In "Claim Rejections - 35 USC § 112" item 4 on page 2 of the above-identified Office Action, claim 12 has been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that there is insufficient antecedent basis for the limitation "the group" in the claims.

In "Claim Rejections - 35 USC § 112" item 5 on page 2 of the above-identified Office Action, claim 15 has been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner states that there is insufficient antecedent basis for the limitation "the processing unit" in the claims.

Accordingly, claims 4, 9, 10, 12, and 15 have been amended to show sufficient antecedent basis. Support for these changes may be found in claims 1, 11, and 22 of the instant application.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The

changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In "Claim Rejections - 35 USC § 102" item 6 on page 3 of the above-identified Office Action, claims 1 and 12 have been rejected as being fully anticipated by the November 1998 publication of "Processor-Based Built-In Self-Test for Embedded DRAM" in vol. 33, No. 11 of the IEEE Journal of Solid-State Circuits by *Dreibelbis, et al.* (hereinafter DREIBELBIS) under 35 U.S.C. § 102(b).

In "Claim Rejections - 35 USC § 103" item 7 on page 4 of the above-identified Office Action, claims 2, 3, 13, and 14 have been rejected as being obvious over **DREIBELBIS** in view of U.S. Patent No. 5,337,318 to *Tsukakoshi, et al.* (hereinafter **TSUKAKOSHI**) under 35 U.S.C. § 103(a).

In "Claim Rejections - 35 USC § 103" item 8 on page 5 of the above-identified Office Action, claims 4-10 and 15-21 have been rejected as being obvious over **DREIBELBIS** under 35 U.S.C. § 103(a).

These rejections have been noted and the claims have been amended in an effort to even more clearly define the

invention of the instant application. Support for the changes is found on page 6 of the specification of the instant application. Additional support may be derived from originally filed claims 1, 11, and 22.

In "Claim Rejections - 35 USC § 103" item 9 on page 7 of the above-identified Office Action, claims 11 and 22 have been rejected as being obvious over **DREIBELBIS** in view of U.S. Patent No. 6,445,627 to *Nakahara, et al.* (hereinafter **NAKAHARA**) under 35 U.S.C. § 103(a).

Applicants respectfully note that **NAKAHARA** has a United States filing date of **June 22, 2001**. See 35 U.S.C. § 102(e). As set forth in the Declaration of record, the instant application claims international priority of the German Application No. **100 63 627.6**, filed **Decemeber 20, 2000**, under 35 U.S.C. § 119. Pursuant to 35 U.S.C. §§ 119, 120 and 363, applicants are entitled to the priority date of the German application. See MPEP §§ 201.13 and 1895. Thus, the instant application predates **NAKAHARA** by more than 5 months. Because **NAKAHARA** was filed after the priority date of the instant application, applicants respectfully believe that **NAKAHARA** is unavailable as prior art.

Applicants acknowledge that perfection of priority can only be obtained by filing a certified English translation of the German priority application. See 35 U.S.C. § 119. On January 31, 2002, applicants filed a Claim for Priority including a certified copy of German application **100 63 627.6** and concurrent herewith files a certified English translation of same.

Accordingly, applicants respectfully believe that priority has been perfected and **NAKAHARA** is unavailable as prior art. Therefore, applicants respectfully submit that the Section 103(a) rejection in item 9 on page 7 of the above-identified Office Action is now moot.

In light of the above, applicants have amended independent claims 1 and 12 with the limitations found in claims 11 and 22 and now believes that none of the references, whether taken alone or in any combination, either show or suggest the features of independent claims 1 and 12. Claims 1 and 12 are, therefore, believed to be patentable over the art.

Before discussing the remaining prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, an integrated circuit including:

a buffer memory having registers for storing data for a connected data processing unit; and

a setting memory connected to the buffer memory, the setting memory **having at least one electrical fuse being written to and read from through the buffer memory.**

Independent claim 12 contains similar language.

The **DREIBELBIS** reference discloses a data processing unit connected to a buffer memory having registers for storing data for said data processing unit. The data stored in this buffer can be read out to indicate which fuses are to be blown to facilitate repair of the memory. **DREIBELBIS** teaches that the data in the buffer memory is serially passed to a fuser. As is known to a person of skill in the art, a fuser is an external device used to blow fuse elements on the integrated circuit. The fuser normally receives the repair information indicating which memory cells of an integrated circuit should be replaced by redundant memory cells from a testing device.

Applicants agree with the Examiner's determination on page 7 of the above-identified Office Action that **DREIBELBIS** "does not specifically teach" electrical fuses as recited in claims 1 and 12 of the instant application.

In further contrast to the present invention, **DREIBELBIS does not show** that the buffer memory provides dual functionality by first providing memory space for the internal data processing unit and second providing the capability to write to or to read from the setting memory as recited in claims 1 and 12 of the instant application.

Clearly, **DREIBELBIS** does not show "a buffer memory **having registers for storing data** for said data processing unit … and **a setting memory** … being at least one of **written to and read from through said buffer memory**" as recited in claim 1 of the instant application. Nor does **DREIBELBIS** teach or suggest a "setting memory having at least one electrical fuse" as recited in claim 1 of the instant application. Claim 12 contains similar language.

The **TSUKAKOSHI** reference discloses a testing apparatus for a memory IC with a redundancy circuit that includes a setting memory to activate redundant memory elements. The proposed combination of **TSUKAKOSHI** and **DREIBELBIS** do not overcome the previously described deficiencies in the cited references by showing a dual functionality to the buffer memory. More specifically, the proposed combination of **TSUKAKOSHI** and **DREIBELBIS do not show** that the buffer memory provides a dual

buffer memory functionality thereby saving a substantial amount of space on the integrated circuit.

In contrast, the present invention claims a buffer memory that may first provide memory space for the internal data processing unit and second provide the capability to write to or to read from the setting memory as recited in claims 1 and 12 of the instant application.

Clearly, **TSUKAKOSHI** does not show a "a buffer memory **having registers for storing data** for said data processing unit ... and **a setting memory** ... being at least one of **written to and read from through said buffer memory**" as recited in claim 1 of the instant application. Nor does **TSUKAKOSHI** teach or suggest a "setting memory having at least one electrical fuse" as recited in claim 1 of the instant application. Claim 12 contains similar language.

The **NAKAHARA** reference discloses a semiconductor integrated circuit that efficiently repairs a defective bit in a memory. A setting circuit in **NAKAHARA** sets an identification code and information corresponding to the identification code and serially outputs the set information. **NAKAHARA** indicates that the setting circuit also controls the fuse macro cells.

NAKAHARA does not show that the buffer memory provides dual functionality by first providing memory space for the internal data processing unit and second providing the capability to write to or to read from the fused setting memory as recited in claims 1 and 12 of the instant application.

Clearly, **NAKAHARA** does not show "a buffer memory **having registers for storing data** for said data processing unit … and **a setting memory … having at least one electrical fuse** being at least one of **written to and read from through said buffer memory**" as recited in claim 1 of the instant application.

In addition, **NAKAHARA** is not available to be cited against the instant application, since the U.S. filing date of June 22, 2001 is subsequent to the effective U.S. filing date of December 20, 2000 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or claim 12. Claim 1 and claim 12 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable

as well because they all are ultimately dependent on either claim 1 or claim 12.

In view of the foregoing, reconsideration and allowance of claims 1-10 and 12-21 are solicited. In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099. Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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